On page 10, after the paragraph which begins on line 3, insert the following paragraph:

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FIG. 10D is a chart showing the values of components in the schematic diagrams depicted in **FIGS. 10A-C**.

On page 22, replace the paragraph starting on line 6 with the following paragraph:

Turning to the input / transmitter side, a first input signal is provided to an input signal interface 204. The input signal is a wideband digital signal, either electrical or optical, according to a variety of signal types (including TCP/IP, Fast Ethernet, SONET, ATM, or other signal types known in the art, on various physical layers such as STS-3, STS-12, OC-3, or OC-12). Various electrical or fiber optic cable connectors may be received by the input signal interface 204 depending on design requirements. Upon receipt

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of the digital input signals, these signals are provided to a regenerator 206. The regenerator 206 preferably includes an input signal amplifier 207, either a limiting amplifier or an automatic gain control, to provide gain, as necessary, and smooth out variations in input signal amplitude either a limiting amplifier 207 or automatic gain control 208 to provide gain, as necessary, and smooth out variations in input signal amplitude. The regenerator 206 further includes a first clock / data recovery circuit 210 to provide protocol independence. The first clock and data recovery circuit 210 includes at least one oscillator 212, such as a crystal, to regulate the clock frequencies. When more than one oscillator is provided, the integrated circuit utilizes two phase locked loops to permit modulation as different frequencies, so as to accommodate more than one data transmission protocol, such as TCP/IP, Fast Ethernet, SONET, and ATM. Thus, a single transceiver 200 is

enabled to transmit and receive more than one of the aforementioned protocols. Switching between clock frequencies may be performed by manually substituting an existing oscillator 212 with an oscillator of a different frequency. More preferably, as shown in **FIG. 8**, multiple oscillators 212, 213 may be built into the transceiver 200, and a switch 214 may accomplish switching between the oscillators 212, 213. This switching may be controlled manually, or, more preferably, by a controller 250, such as by using transistor-transistor logic. Either oscillator 212, 213 provides a clock signal to the data recovery electronics 215.

On page 24, replace the paragraph starting on line 3 with the following paragraph:

Turning to the output/receiver side, an incident laser beam is received by the laser receiving module 229 and converted to a preamplified electrical signal. The signal is provided to output signal electronics 230, which includes several elements. First the signal is provided to a second regenerator 232. The regenerator 232 preferably includes a signal amplifier 234, either a limiting amplifier or an automatic gain control, to provide gain, as necessary, and smooth out variations in signal amplitude. The second regenerator 232 preferably further includes a second clock / data recovery unit 236. The second clock and data recovery unit 236 preferably also comprises a switchable dual oscillator such as the dual oscillator 212, 213 shown in connection with the first clock and date recovery unit 210, and operates in a similar manner. Upon regeneration, the resulting digital electronic signal may be provided to an optional de-multiplexer 238 to segregate at least one additional output signal 205. Following de-multiplexing, the digital signal remaining in the output signal electronics 230 is passed to an output signal interface 240. An output signal

interface 240 converts the electronic signal into an appropriate output signal, such as an electronic or optical signal. Either electrical or optical interfaces may be provided, subject to the inclusion of appropriate hardware as would be apparent to one skilled in the art. In one embodiment, the output signal interface 240 includes a fiber transmitter that converts the electronic signal to an optical signal, and further includes a fiber optic connector for connecting a fiber optic cable. The primary output signal is a wideband digital signal, and may be in accordance with various protocols known in the art, including TCP/IP, IPX, Fast Ethernet, SONET, or ATM, and may operate on various physical layers known in the art, including STS-3, STS-12, OC-3, or OC-12. Although depicted separately, the output signal interface 240 and input signal interface 204 may be combined, and if the interfaces 204, 240 include a fiber optic transmitter and a fiber optic receiver, then an integrated fiber optic transceiver may be used.

COMMENTS

Amended Figure 8 and the amendments to the paragraphs located on pages 22 and 24, as indicated above, are submitted to clarify Figure 8 and its associated description. Presently, in Figure 8 reference numerals 207 and 208 refer to the same object and reference numerals 234 and 235 refer to the same object. In each instance, the object being referred to provides gain to a signal and can be either a limiting amplifier or an automatic gain control. The amendment to the specification now identifies each object as a signal amplifier having reference numeral of 207 and 234, respectively, and states that the signal amplifier can be either a limiting amplifier or an automatic gain control. Amended Figure 8 reflects these changes, as reference numerals 208 and 235 have been removed.

Figures 9, 9A, 9B, and 9C have been amended to more clearly illustrate the laser driver circuit. Amended Figure 9 illustrates how the schematic illustrated across Figures 9A and 9B are assembled to form a completed laser driver circuit. The portion of the schematic that was in Figure 9C is now incorporated into amended Figure 9A. The values of the various components have been removed from amended Figures 9A and 9B and have instead been placed on the chart illustrated in amended Figure 9C.

Figures 10, 10A, 10B, 10C, and 10D have been amended to more clearly illustrate the complimentary circuit for the laser driver. Amended Figure 10 illustrates how the schematic illustrated across Figures 9A, 10B, and 10C are assembled to form a completed schematic of the complimentary circuit. The values of the various components have been removed from amended Figures 10A, 10B, and 10C and have instead been placed on the chart illustrated in amended Figure 10D.

Respectfully submitted,

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